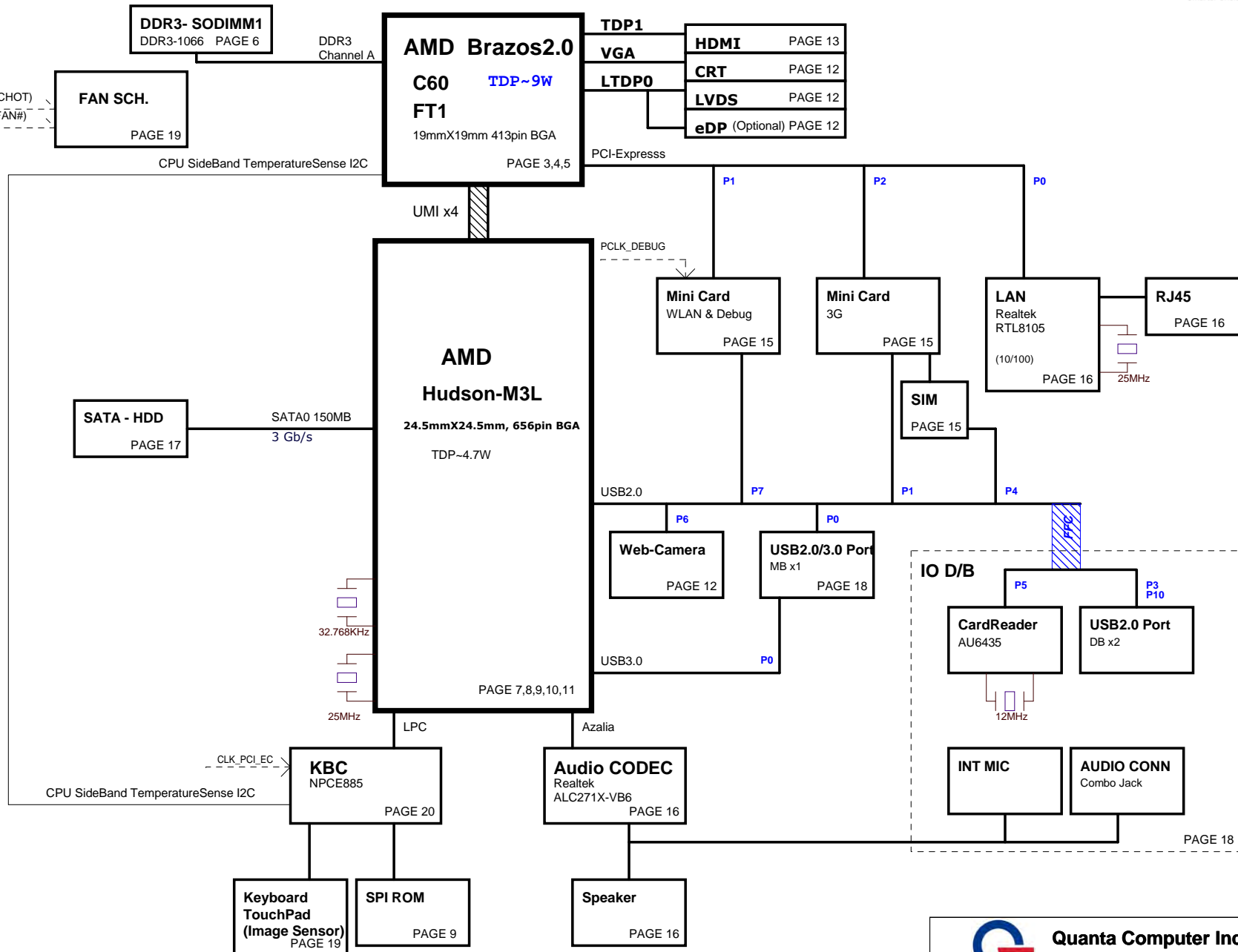


# ZHG SYSTEM DIAGRAM

## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

EDP@ -----> eDP panel  
LVDS@ -----> LVDS panel  
HDT@ -----> HDT function  
3G@ -----> 3G function  
U2@ -----> USB2.0 only  
U3@ -----> USB3.0 function  
885S@ -----> EC885S  
885L@ -----> EC885L



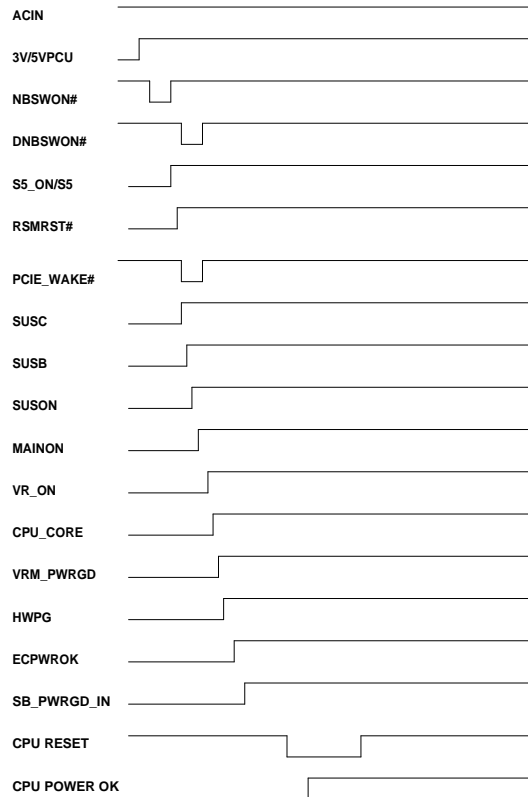
Quanta Computer Inc.

PROJECT : ZHG

Size	Document Number	Rev
	Block Diagram	1A
Date:	Tuesday, January 03, 2012	Sheet 1 of 28

[illegible]

## Power Sequence



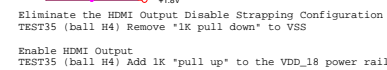
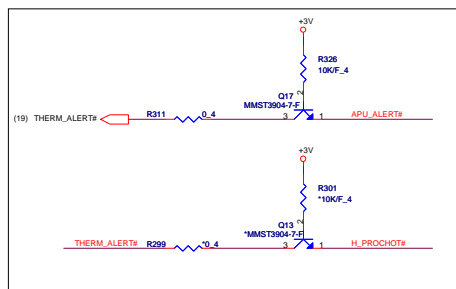
## Hudson M3L SMBUS

A68M SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AE25	DDR / WLAN / 3G / Image Sensor
SCLK1 SDATA1 (+3V_S5)	T7 R7	Not used
SMB_EC_CLK SMB_EC_DAT (+3V_S5)	H19 G19	Charger / Battery
SB_SCLK3 SB_SDATA3 (+3V_S5)	G22 G21	APU

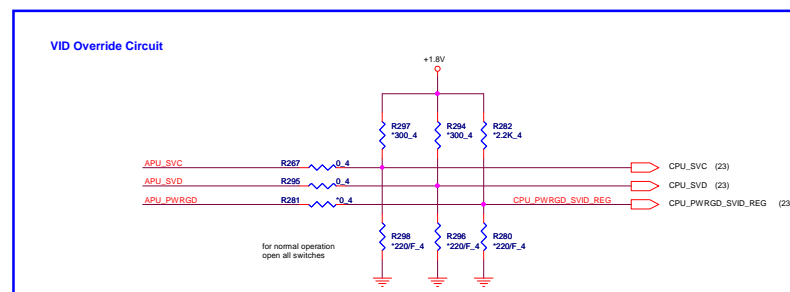
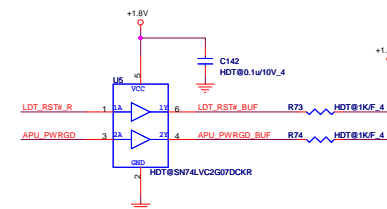
## KBC(EC) SMBUS

NPCE885 SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	70 69	Battery / Charger
APU_SIC_EC APU_SID_EC (+3VPCU)	67 68	APU

This page is different AMD Nile

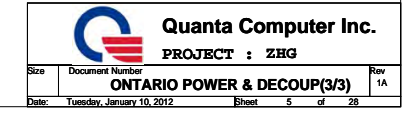


### VID Override Circuit

[illegible]

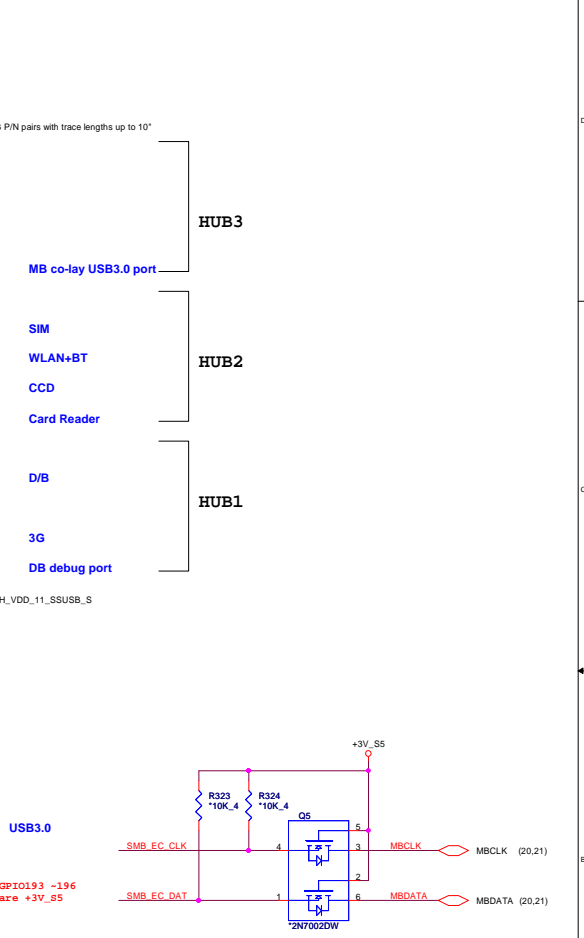
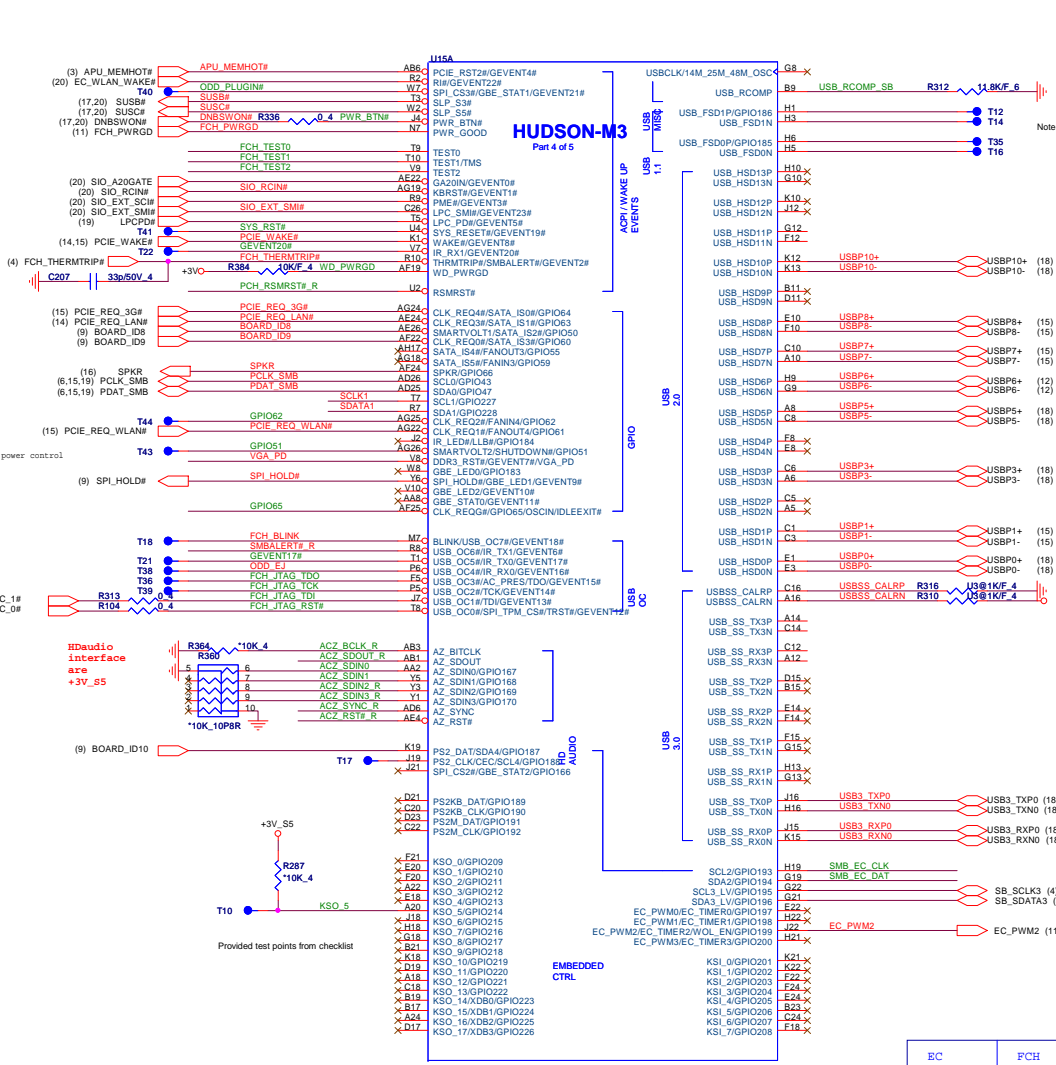
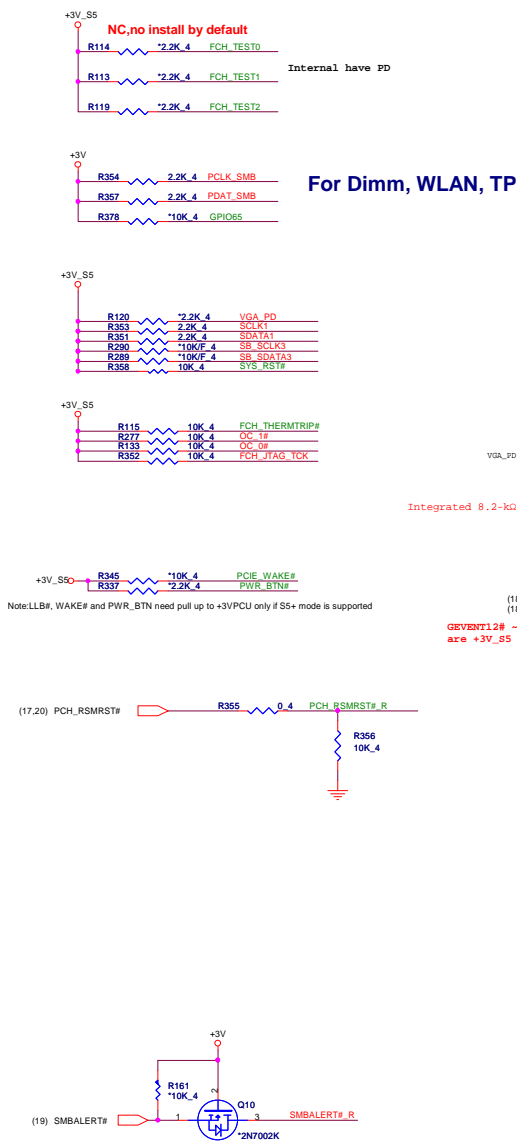
	3	2	1	0	DP AUX+	DP AUX-
HDMI	Clock	CH0	CH1	CH2	DDC Clock	DDC Data
LVDS Panel	Clock	CH0	CH1	CH2	DDC Clock	DDC Data
eDP Panel	ML3	ML2	ML1	ML0	AUX+	AUX-

+V CORE



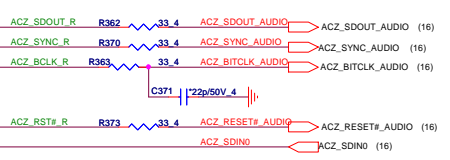


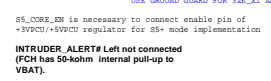
(CLG)



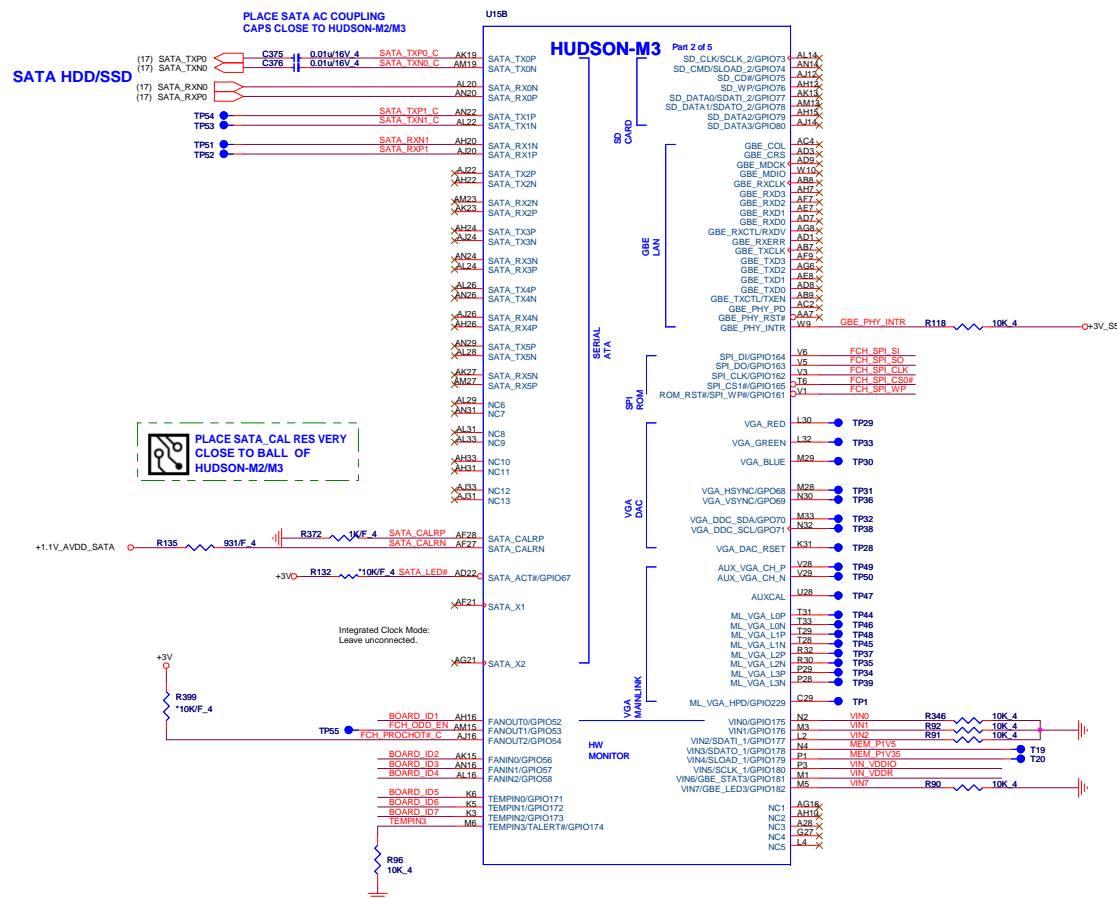
EC	FCH	Device I2C_Device(S)			
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		APU			ALL
I2Ce_3(M)					
	I2Cf_3(M)	APU			S5
	I2Cf_1(M)				S5
	I2Cf_0(M)	DDR	WLAN/3G	Image Sensor	S0

## To Azalia



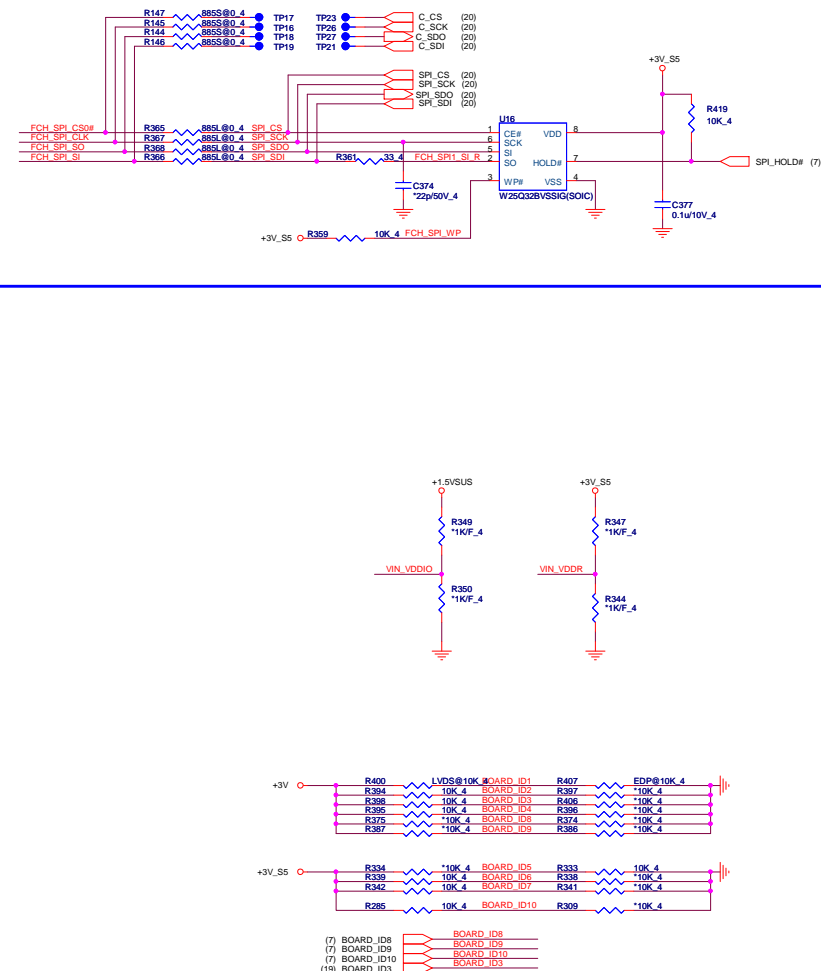


**(CLG)**



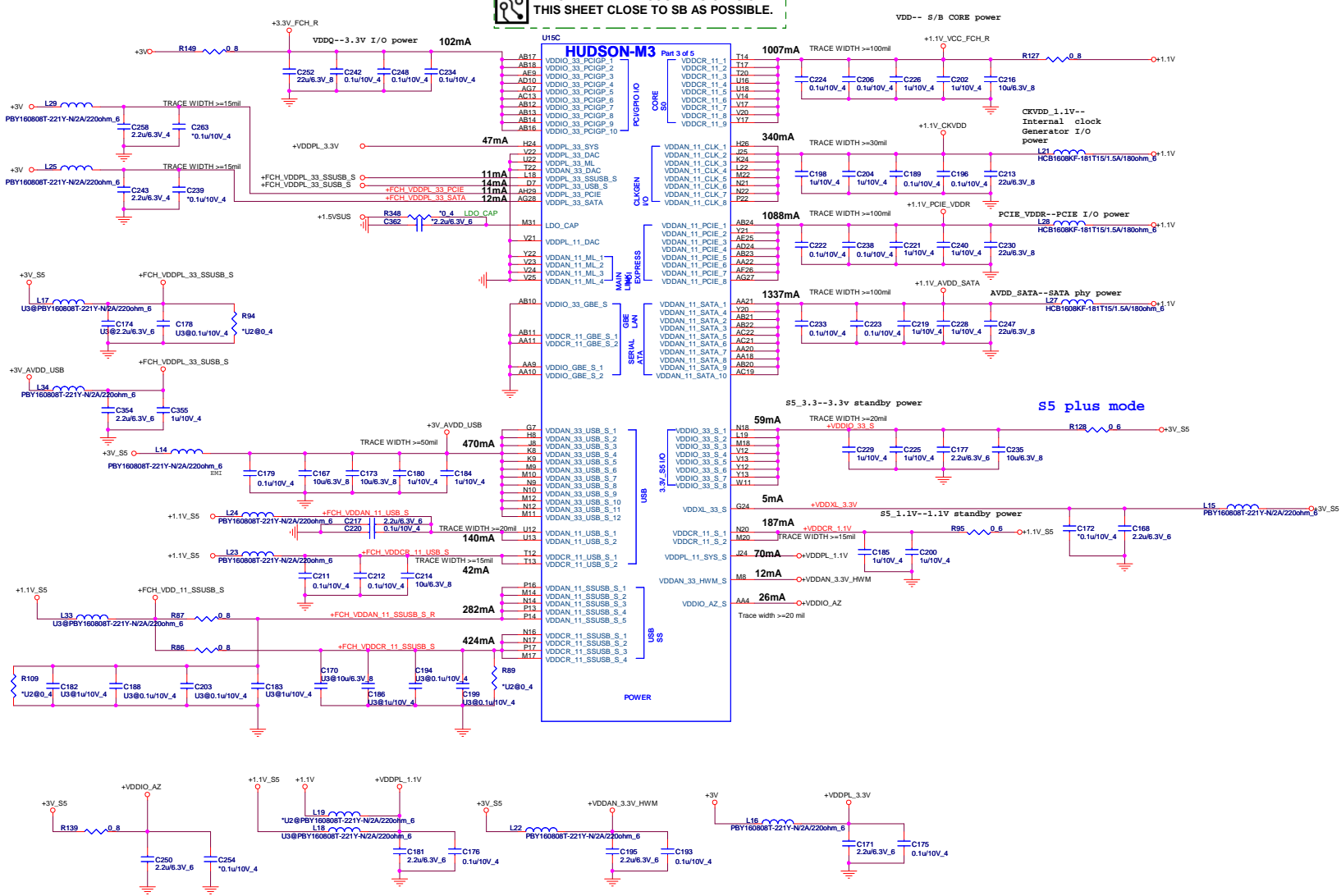
## BOARD ID SETTING

BOARD_ID1	LCD	BOARD_ID3	For TP
0	eDP	0	ELAN
1	LVDS	1	Synaptics



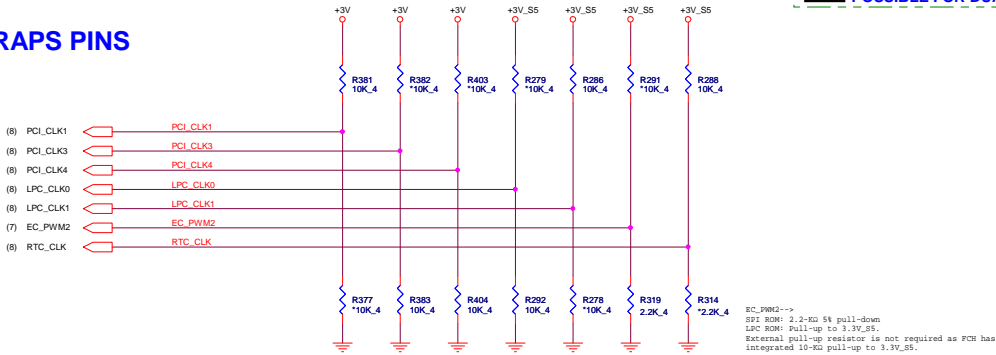


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

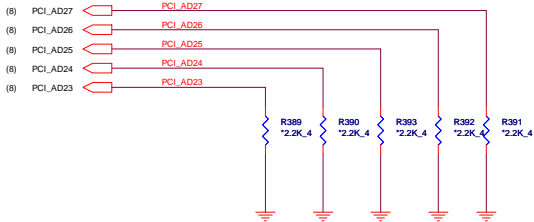


REQUIRED STRAPS

	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

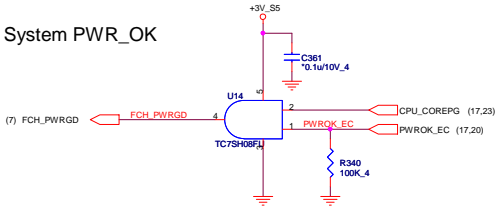
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

System PWR\_OK

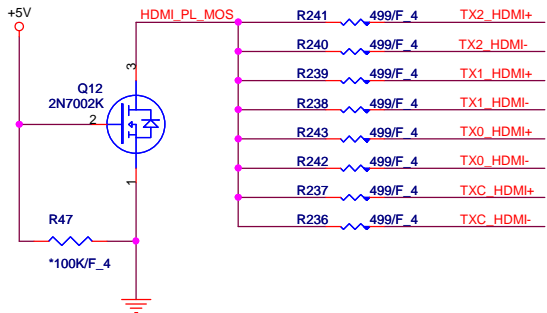


FCH\_PWRGD\_CKT

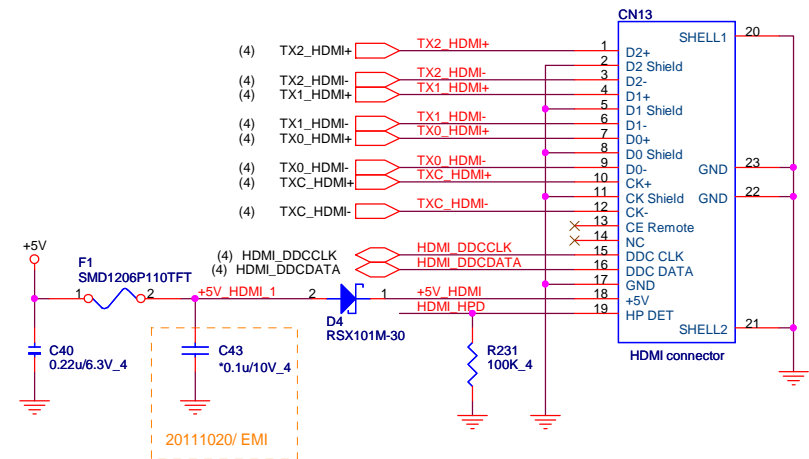
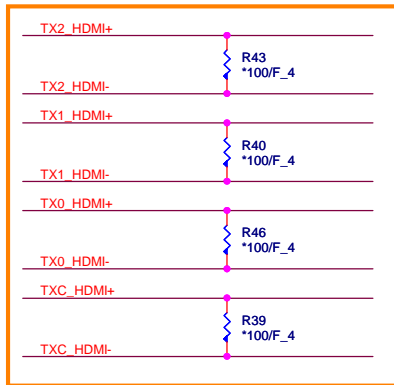


# HDMI (HDM)

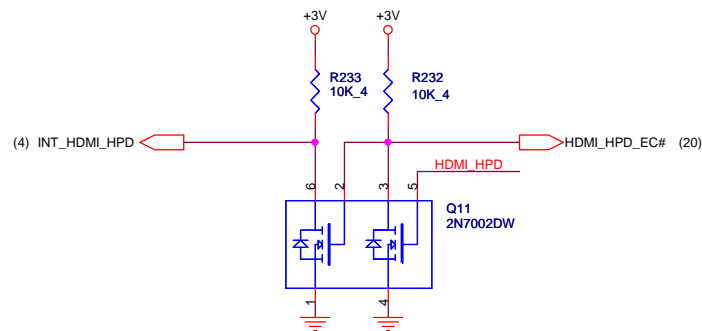
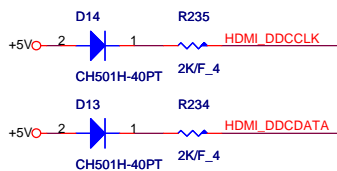
## Close to HDMI Connector



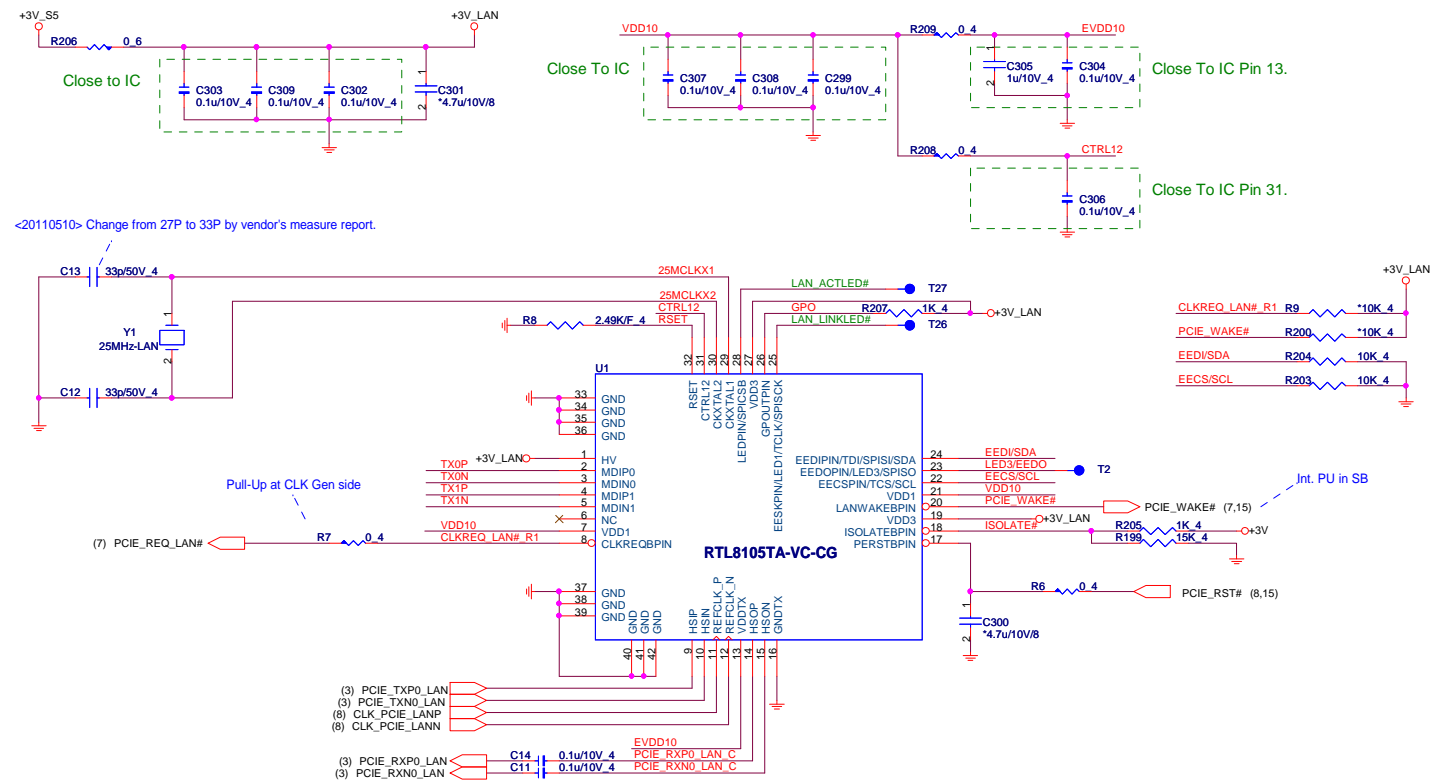
## EMI reserve for HDMI



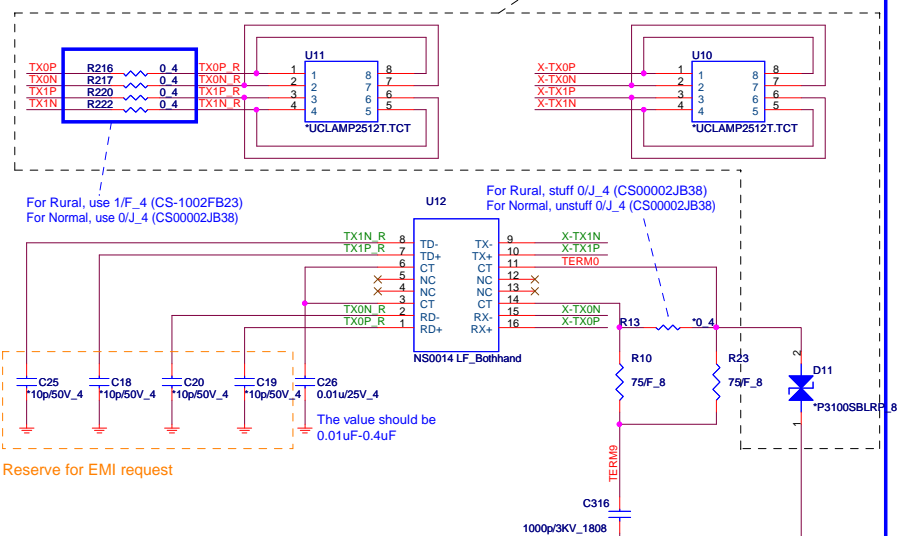
## SDVO I2C Control (HDM)



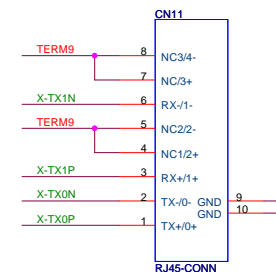
## LAN (LAN)



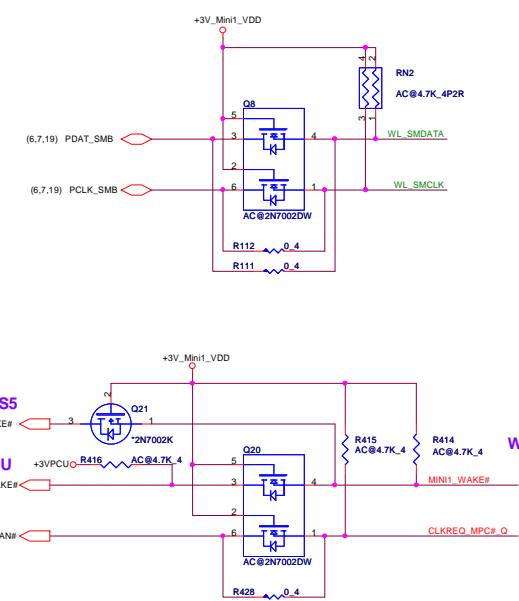
## TRANSFORMER (LAN



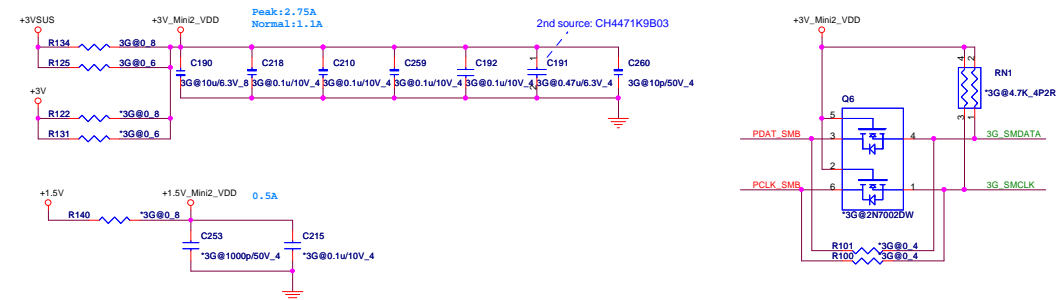
## RJ45 Connector (LAN)



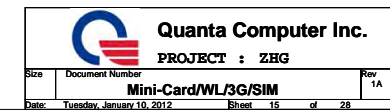
### Mini Card 1 (MPC)



### Mini Card 2 (MNC)

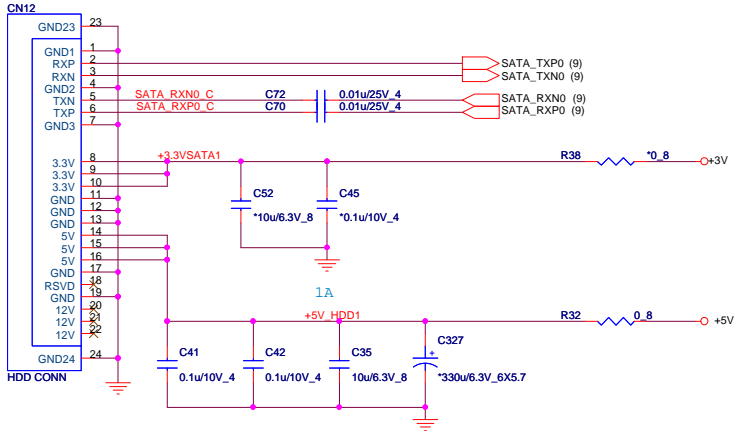


## MultiMedia SIM (MNC)

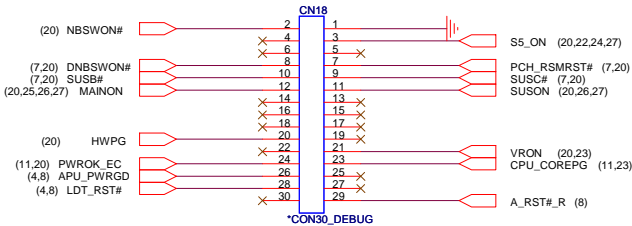




2.5" SATA HDD (HDD)

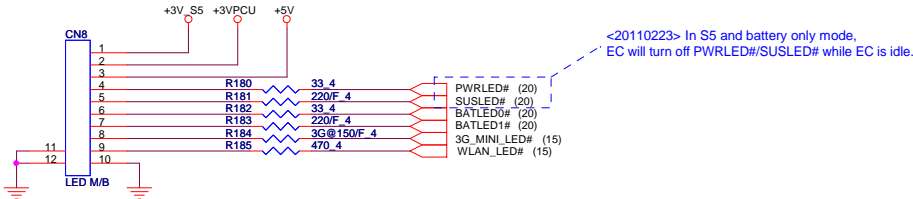


Power Sequence Connector(CPU)

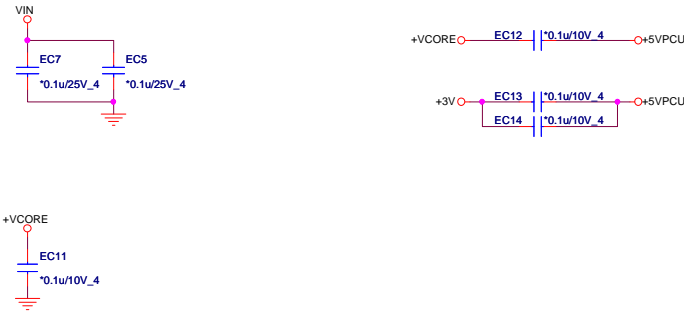


1	GND	11	SUSON	21	VRON
2	NBSWON#	12	MAINON	22	RESERVE
3	S5_ON	13	RESERVE	23	CPU_COREPG
4	RESERVE	14	RESERVE	24	PWROK_EC
5	RESERVE	15	RESERVE	25	RESERVE
6	RESERVE	16	RESERVE	26	APU_PWRGD
7	PCH_RSMRST#	17	RESERVE	27	RESERVE
8	DNBSWON#	18	RESERVE	28	LDT_RST#
9	SUSC#	19	RESERVE	29	A_RST#_R
10	SUSB#	20	HWPG	30	RESERVE

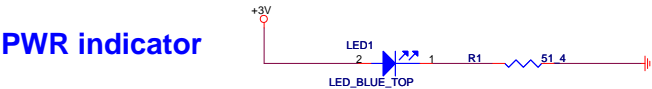
LED DB (UIF)



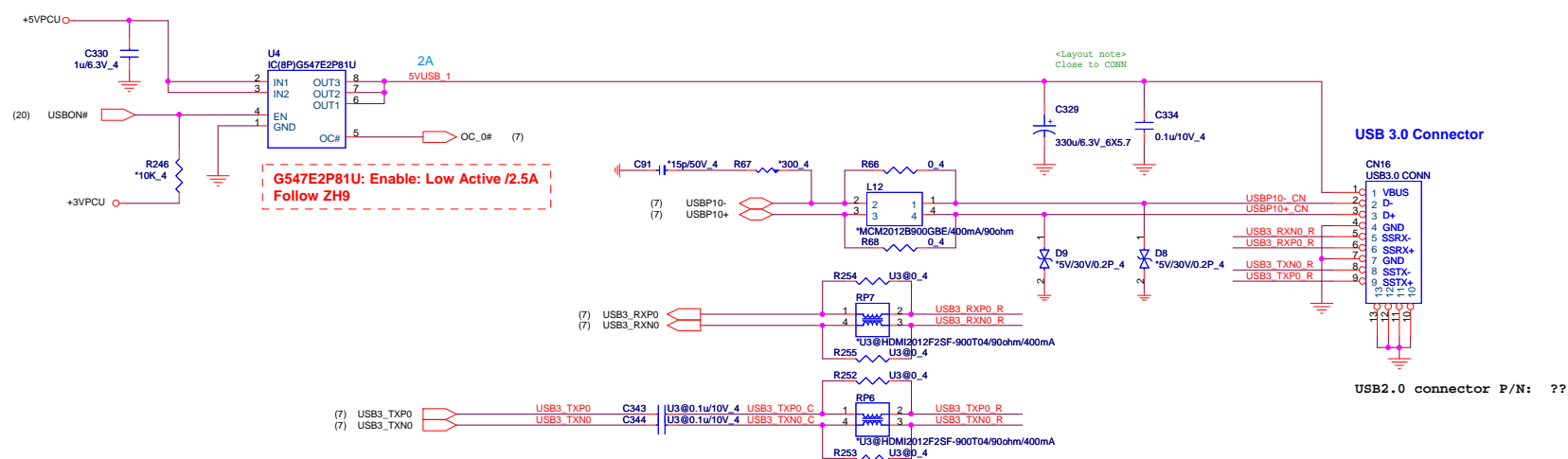
Stitching Cap(EMC)



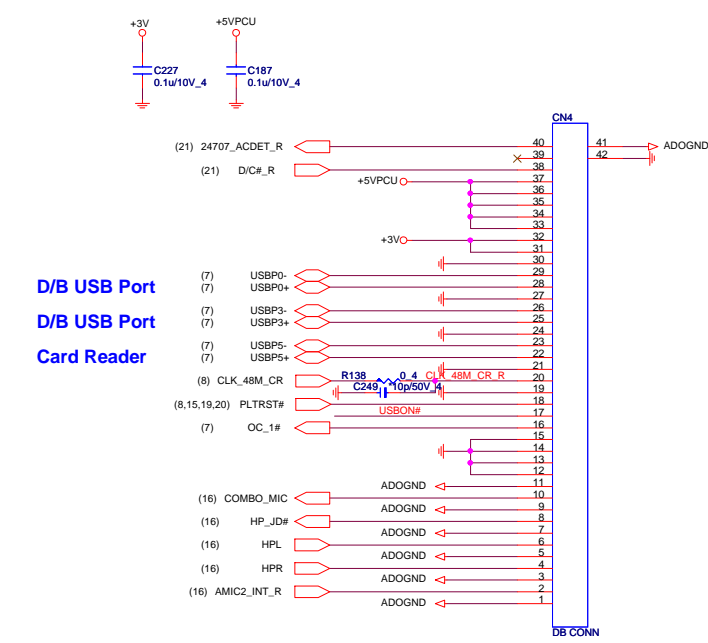
POWER LED(UIF)



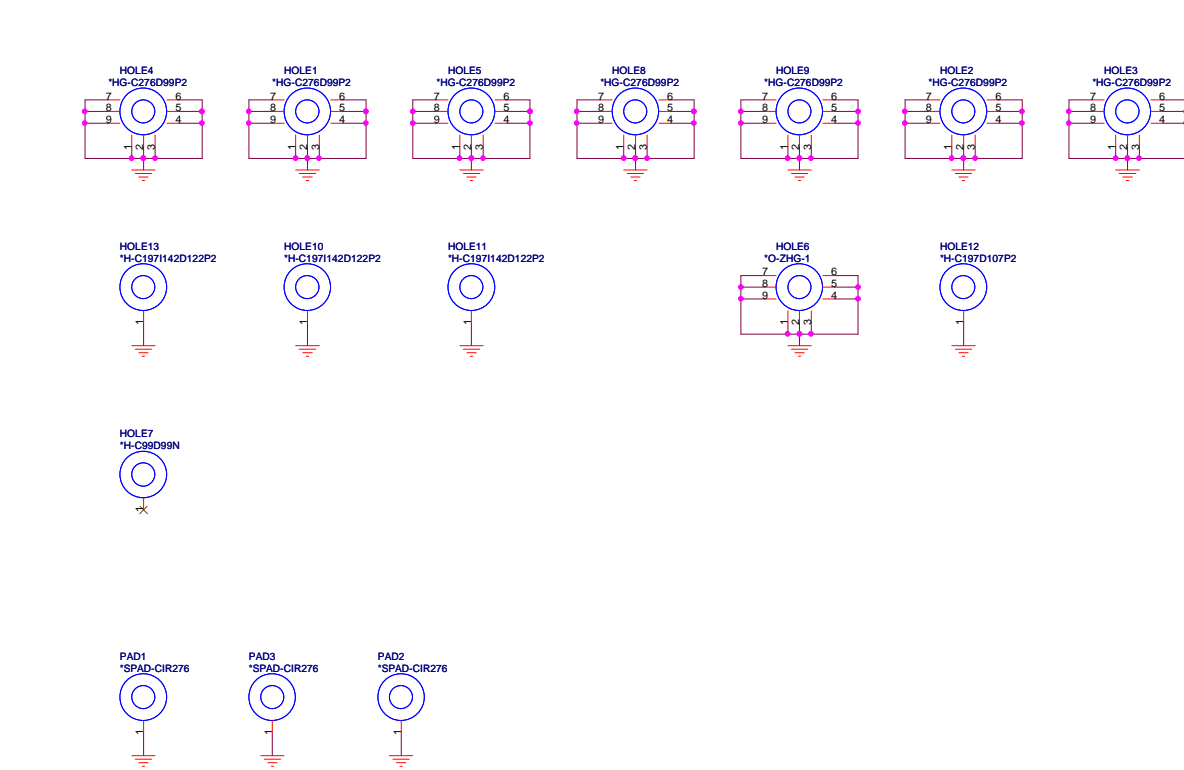
USB Left (USB)



IO D/B (UIF)



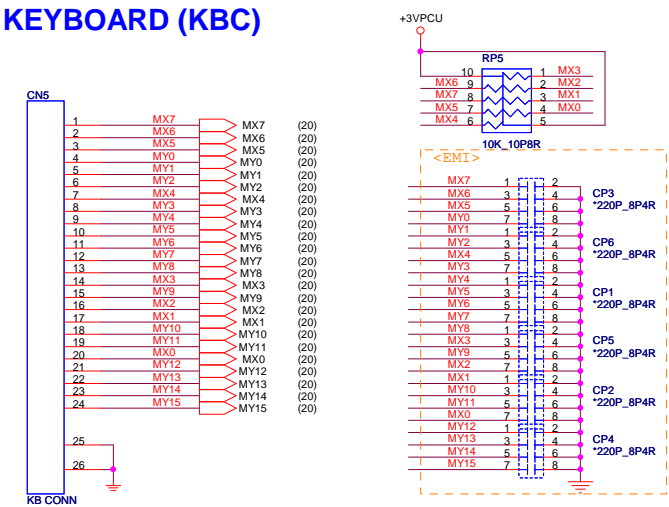
HOLE(OTH)



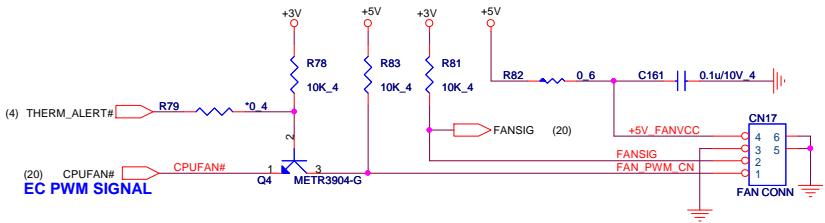
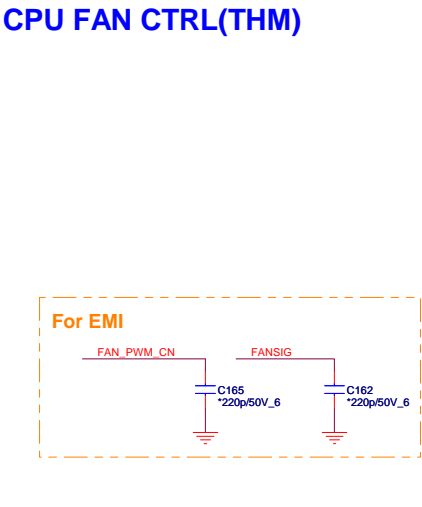
POWER M/B (DCD)



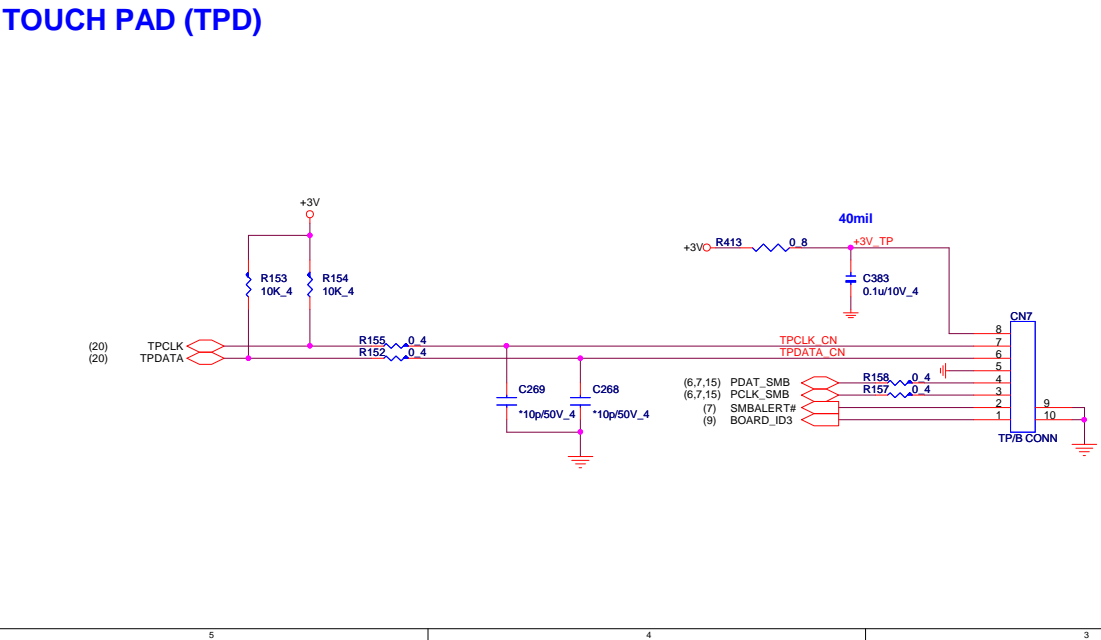
# KEYBOARD (KBC)



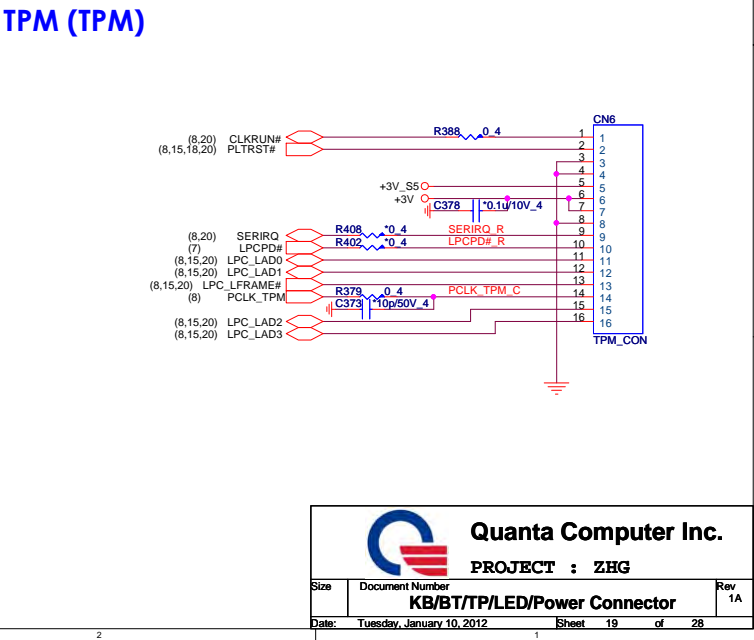
# CPU FAN CTRL(THM)




# TOUCH PAD (TPD)



# TPM (TPM)





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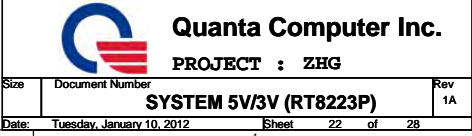
PROJECT : ZHG

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	1A
Date:	Tuesday, January 10, 2012	Sheet 19 of 28

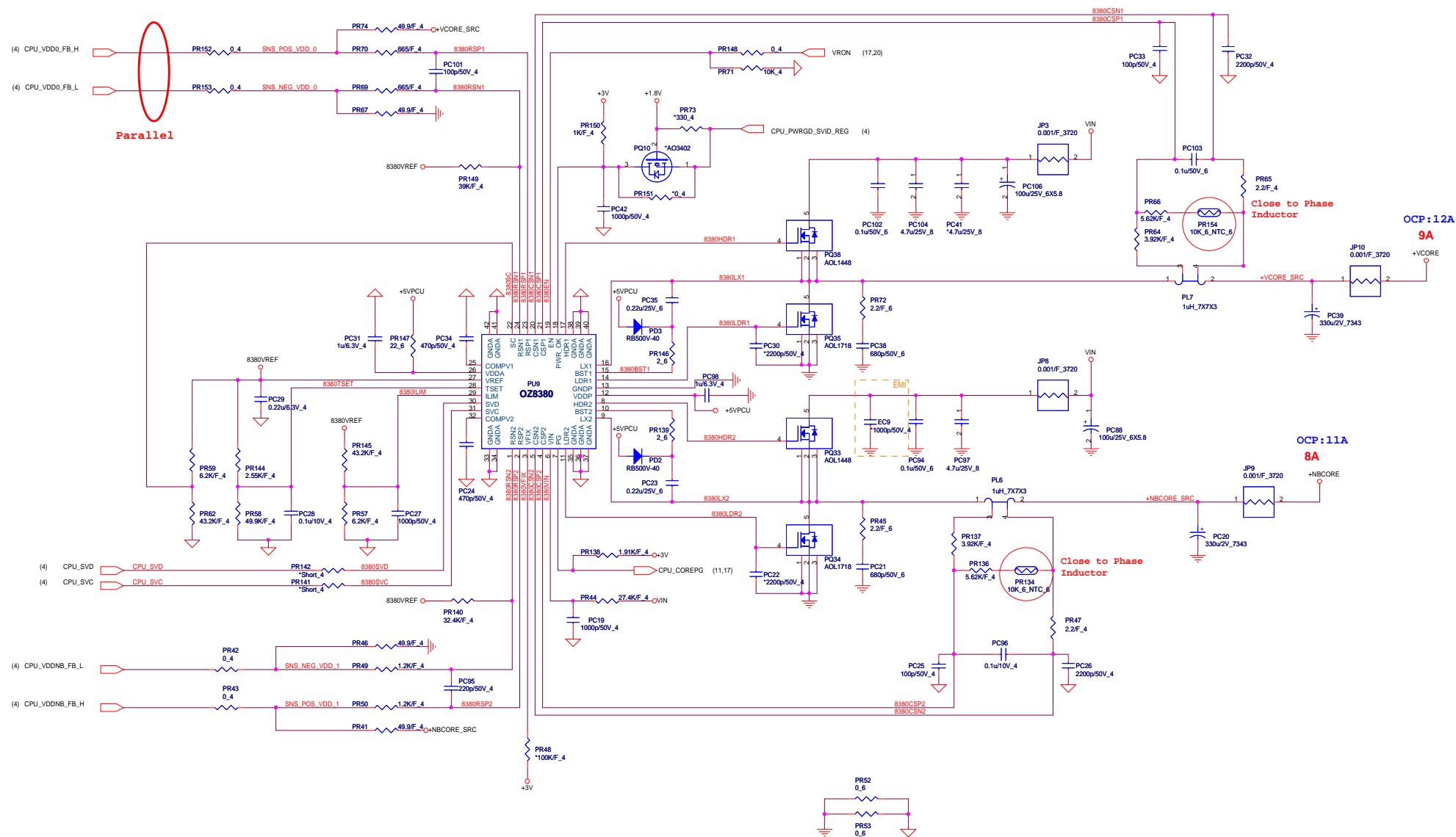




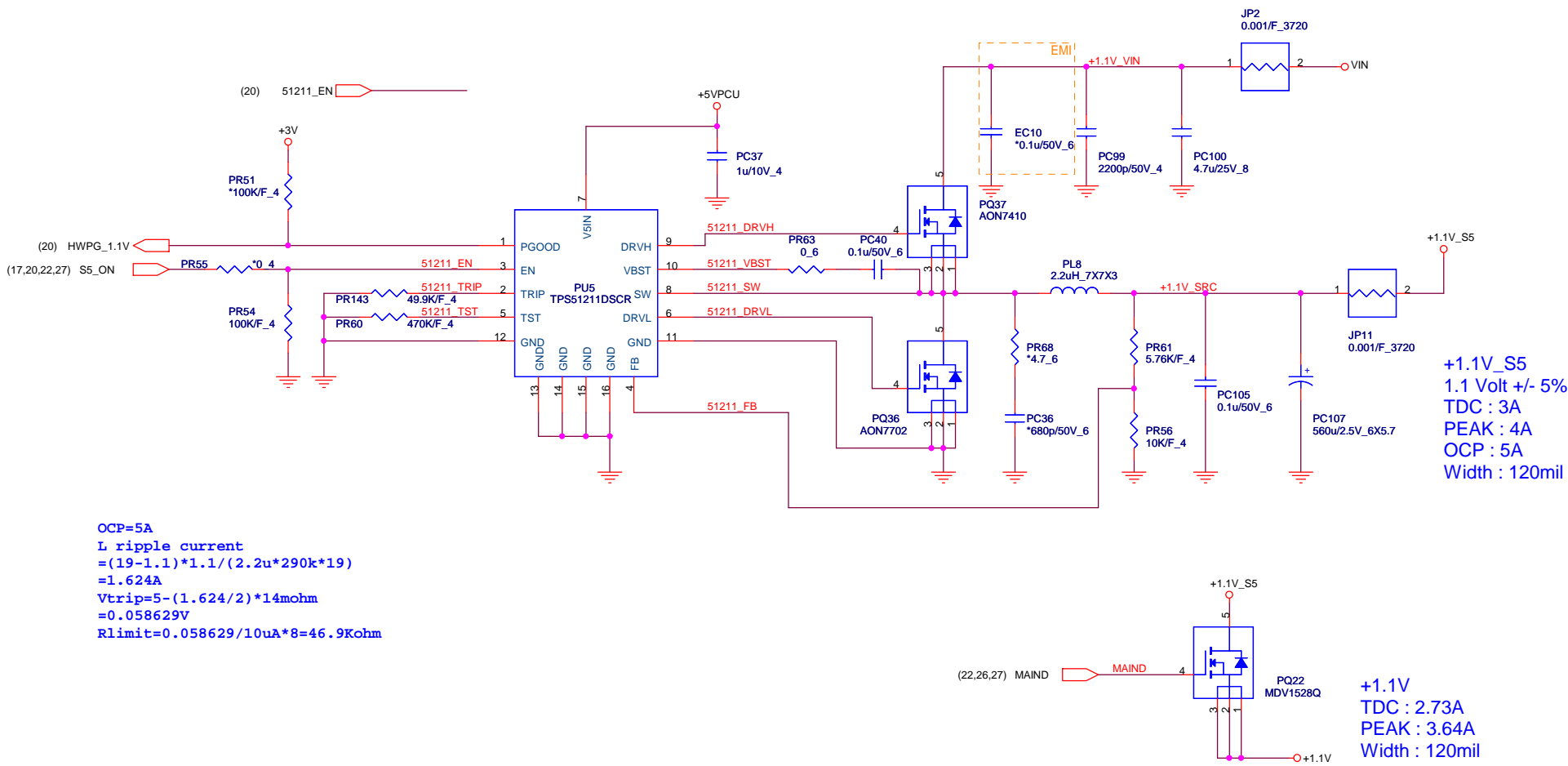
**WWW.AliSaler.Com**



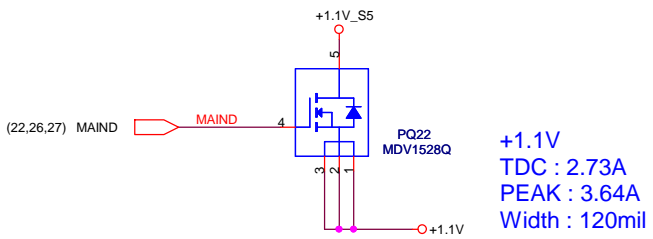
(DCD)




(DCD)



OCP=5A  
L ripple current  
=(19-1.1)\*1.1/(2.2u\*290k\*19)  
=1.624A  
Vtrip=5-(1.624/2)\*14mohm  
=0.058629V  
Rlimit=0.058629/10uA\*8=46.9Kohm

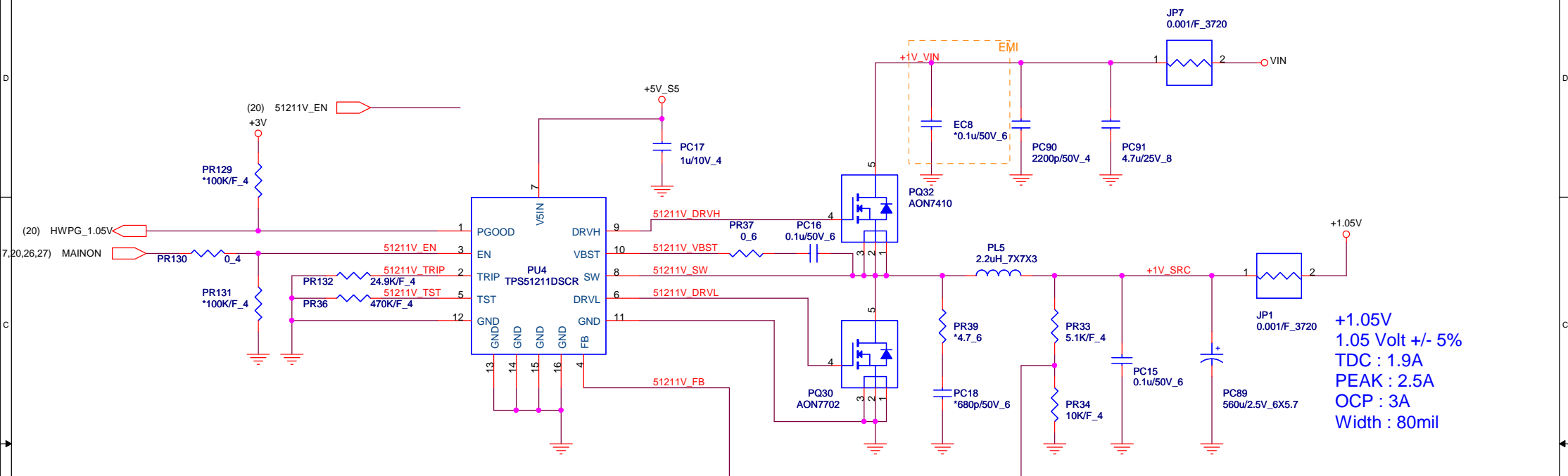




**Quanta Computer Inc.**  
**PROJECT : ZHG**

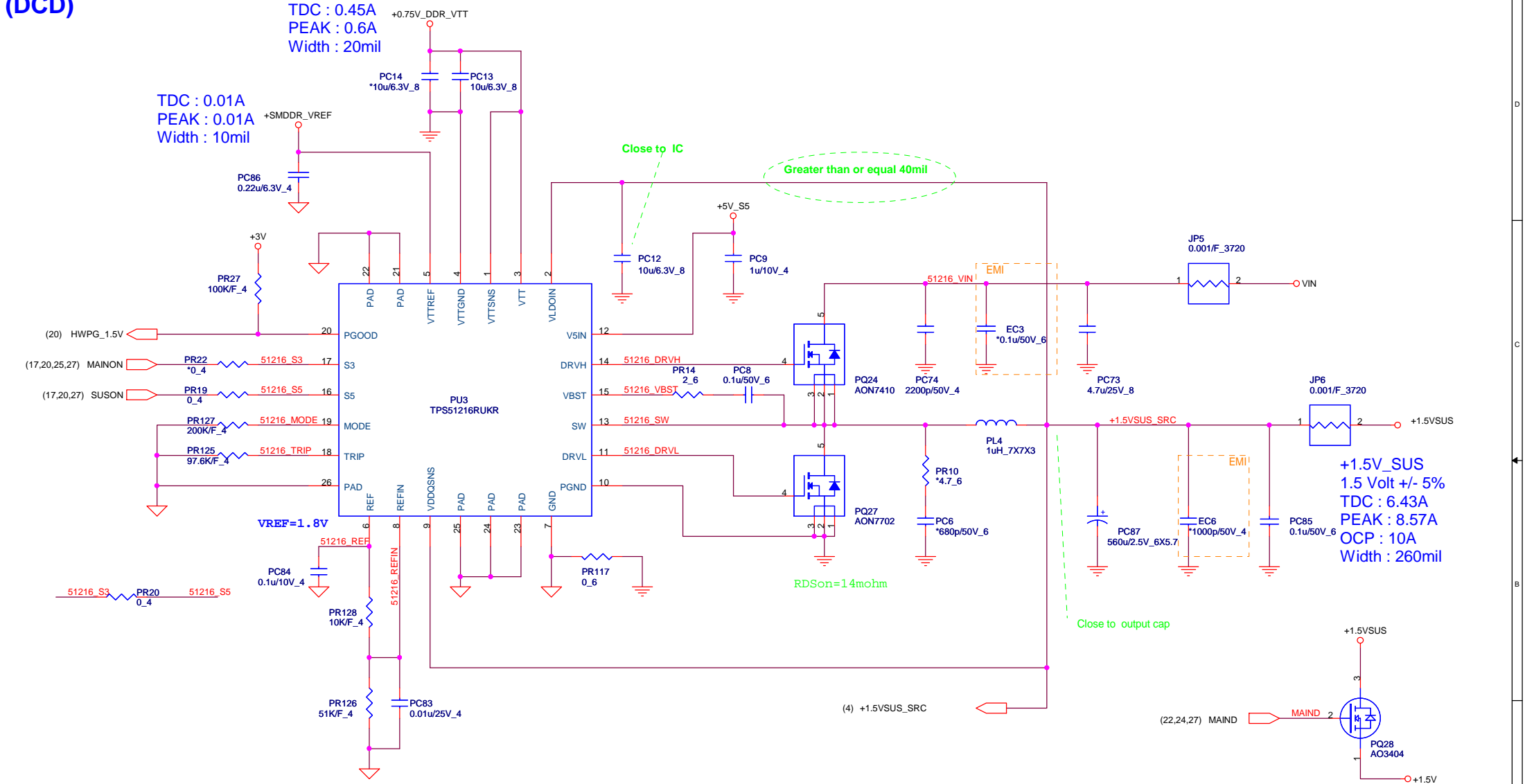
Size	Document Number	Rev
	<b>VCCP 1.1V(TPS51211)</b>	1A
Date:	Wednesday, January 11, 2012	Sheet 24 of 28

**(DCD)**




```
OCP=3A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=3-(1.555/2)*14mohm
=0.03111V
Rlimit=0.03111/10uA*8=24.89Kohm
```

(DCD)



OCP=10A  
I ripple current  
=(19-1.5)\*1.5/(1u\*400k\*19)  
=3.454A  
Vtrip=10-(3.454/2)\*14mohm  
=0.1158V  
Rlimit=0.1158/10uA\*8=92.657Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

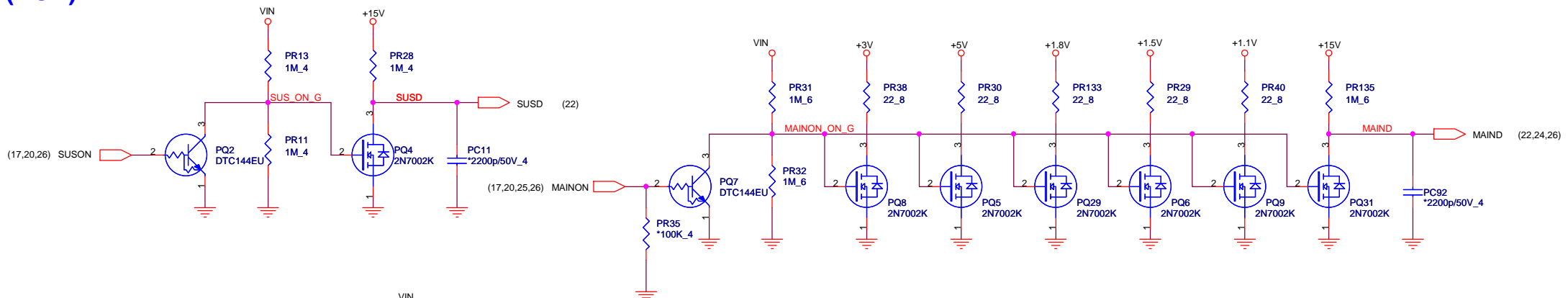


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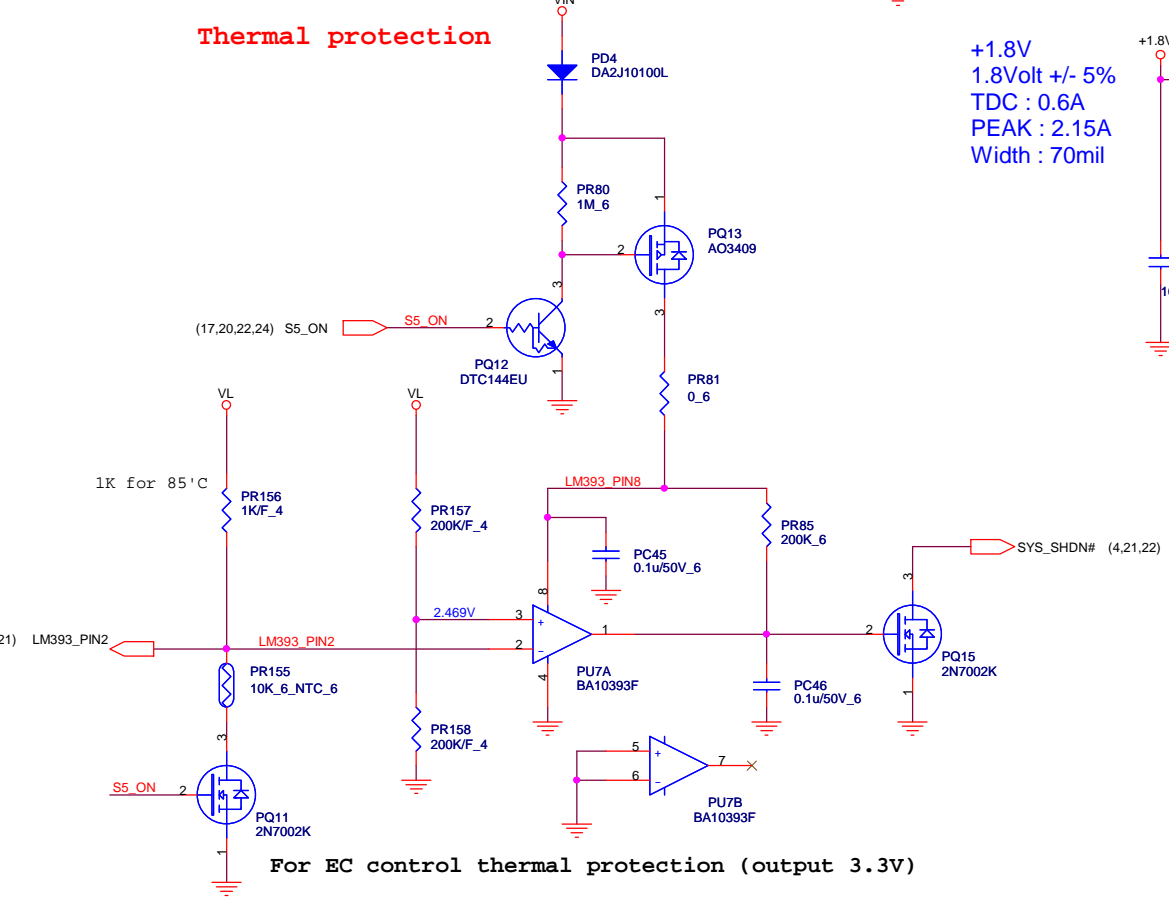
PROJECT : ZHG

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
Date:	Tuesday, January 10, 2012	Sheet 26 of 28

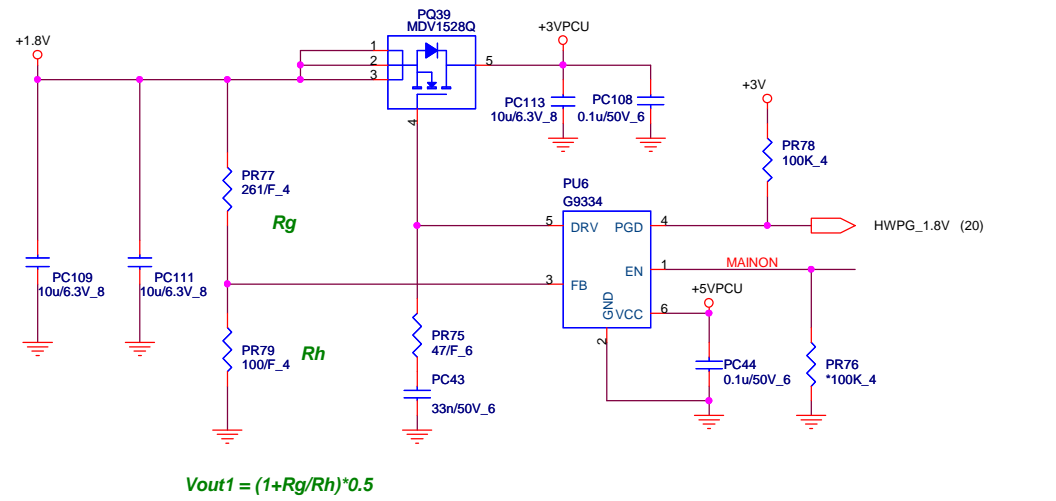
(DCD)




Thermal protection



+1.8V  
1.8Volt +/- 5%  
TDC : 0.6A  
PEAK : 2.15A  
Width : 70mil





**Quanta Computer Inc.**  
PROJECT : ZHG

Size	Document Number	Rev
Discharge /Thermal protection		1A
Date:	Tuesday, January 10, 2012	Sheet 27 of 28

APPROVED BY: Edison Huang CHECK BY: Kevin